#3

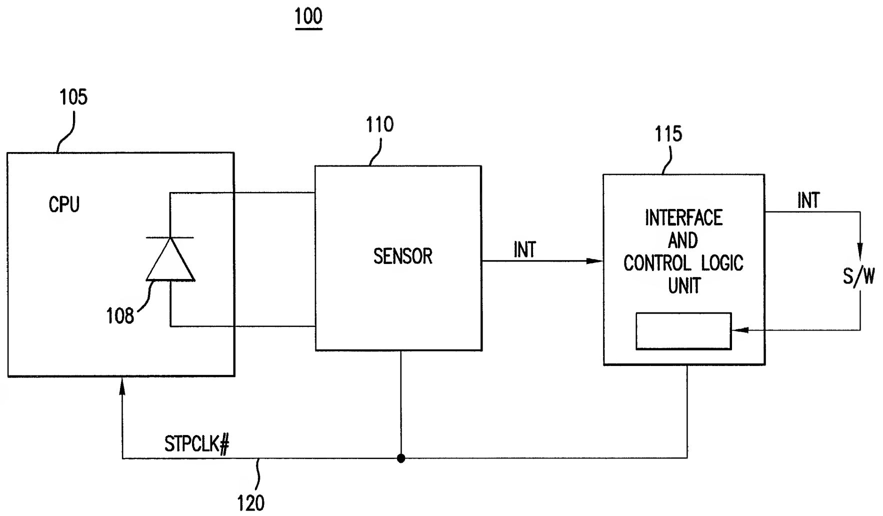

100
105
CPU
108
110
SENSOR
INT
115
INTERFACE AND CONTROL LOGIC UNIT
INT
S/W
STPCLK#
120

FIG.1

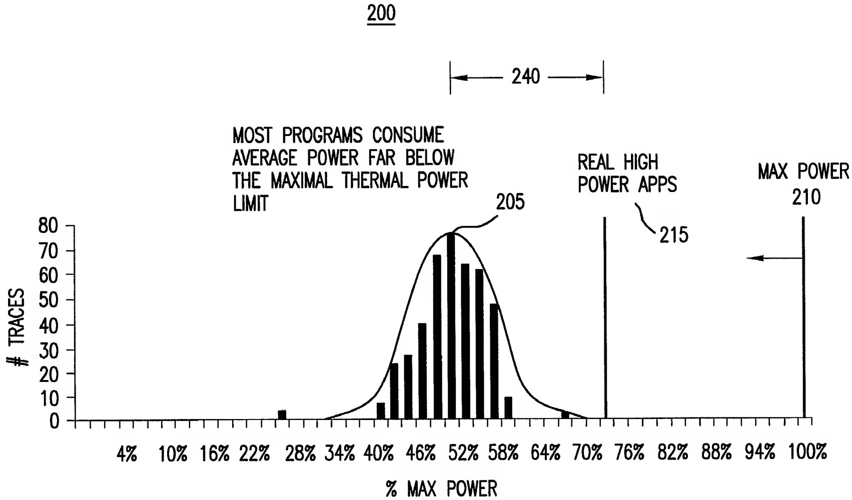

200
240
MOST PROGRAMS CONSUME AVERAGE POWER FAR BELOW THE MAXIMAL THERMAL POWER LIMIT
205
REAL HIGH POWER APPS
215
MAX POWER
210
TRACES
80
70
60
50
40
30
20
10
0
4%
10%
16%
22%
28%
34%
40%
46%
52%
58%
64%
70%
76%
82%
88%
94%
100%
% MAX POWER

FIG.2

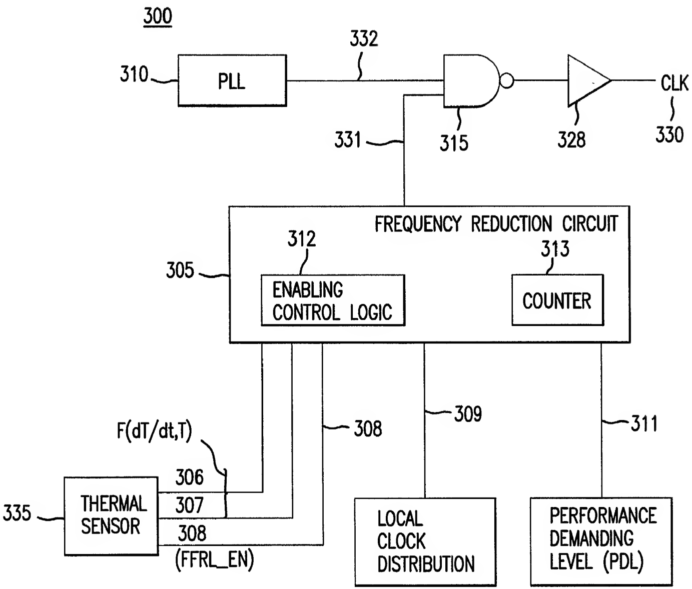

300
310
PLL
332
315
328
CLK
330
331
305
FREQUENCY REDUCTION CIRCUIT
312
ENABLING CONTROL LOGIC
313
COUNTER
F(dT/dt,T)
308
309
311
335
THERMAL SENSOR
306
307
308
(FFRL_EN)
LOCAL CLOCK DISTRIBUTION
PERFORMANCE DEMANDING LEVEL (PDL)

FIG.3

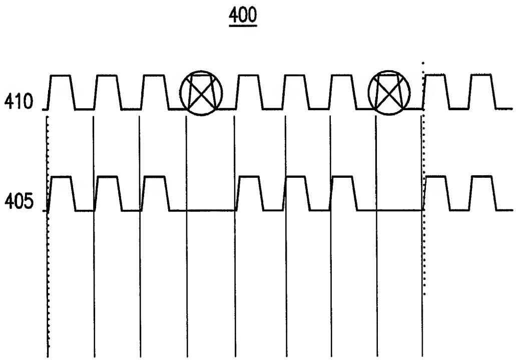


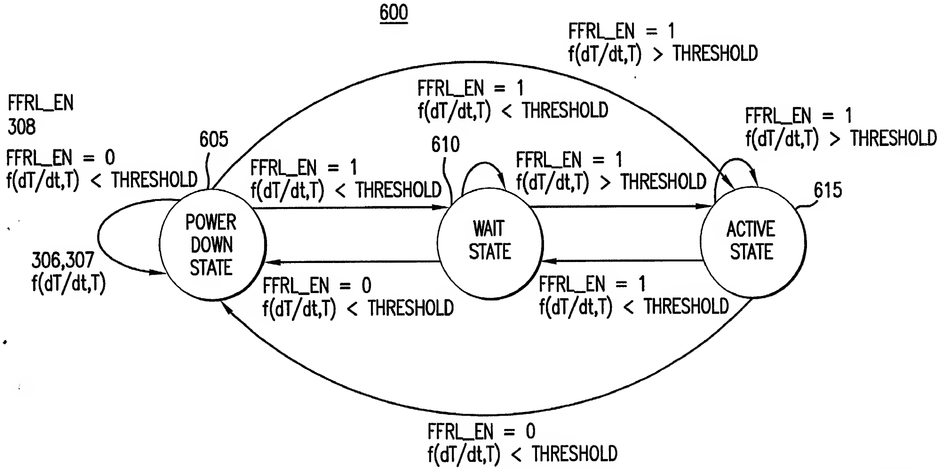
FIG.4

500

FFRL_EN	dT/dt	THERMAL TEMPERATURE	CURRENT LOGIC STATE	PREV. LOGIC STATE
0 (NOT NEAR MAXIMAL THERMAL LIMIT)	NOT CARE	NOT CARE	POWER DOWN	POWER DOWN
0 (NOT NEAR MAXIMAL THERMAL LIMIT)	NOT CARE	NOT CARE	POWER DOWN	WAIT
0 (NOT NEAR MAXIMAL THERMAL LIMIT)	NOT CARE	NOT CARE	POWER DOWN	ACTIVE
1 (NEAR MAXIMAL THERMAL LIMIT)	<0.2 (SLOW RATE)	<MAX. TEMPERATURE−δt	POWER DOWN	POWER DOWN
1 (NEAR MAXIMAL THERMAL LIMIT)	>0.2 (SLOW RATE)	<MAX. TEMPERATURE−δt	WAIT	POWER DOWN
1 (NEAR MAXIMAL THERMAL LIMIT)	<0.2 (SLOW RATE)	<MAX. TEMPERATURE−δt	POWER DOWN	WAIT
1 (NEAR MAXIMAL THERMAL LIMIT)	>0.2 (SLOW RATE)	<MAX. TEMPERATURE−δt	WAIT	WAIT
1 (NEAR MAXIMAL THERMAL LIMIT)	NOT CARE	>MAX. TEMPERATURE−δt	ACTIVE	POWER DOWN
1 (NEAR MAXIMAL THERMAL LIMIT)	NOT CARE	>MAX. TEMPERATURE−δt	ACTIVE	WAIT
1 (NEAR MAXIMAL THERMAL LIMIT)	NOT CARE	>MAX. TEMPERATURE−δt	ACTIVE	ACTIVE

FIG.5

LOGIC STATES DIAGRAM OF FAST FREQUENCY REDUCTION LOGIC (FFRL)



FFRL_EN: FAST FREQUENCY REDUCTION LOGIC ENABLE SIGNAL; THRESHOLD: LOGIC STATE TRANSITE THRESHOLD; dT/dt: TEMPERATURE CHANGING RATE; T: THERMAL TEMPERATURE; f(dT/dt,T): FUNCTION OF dT/dt AND T

FIG.6